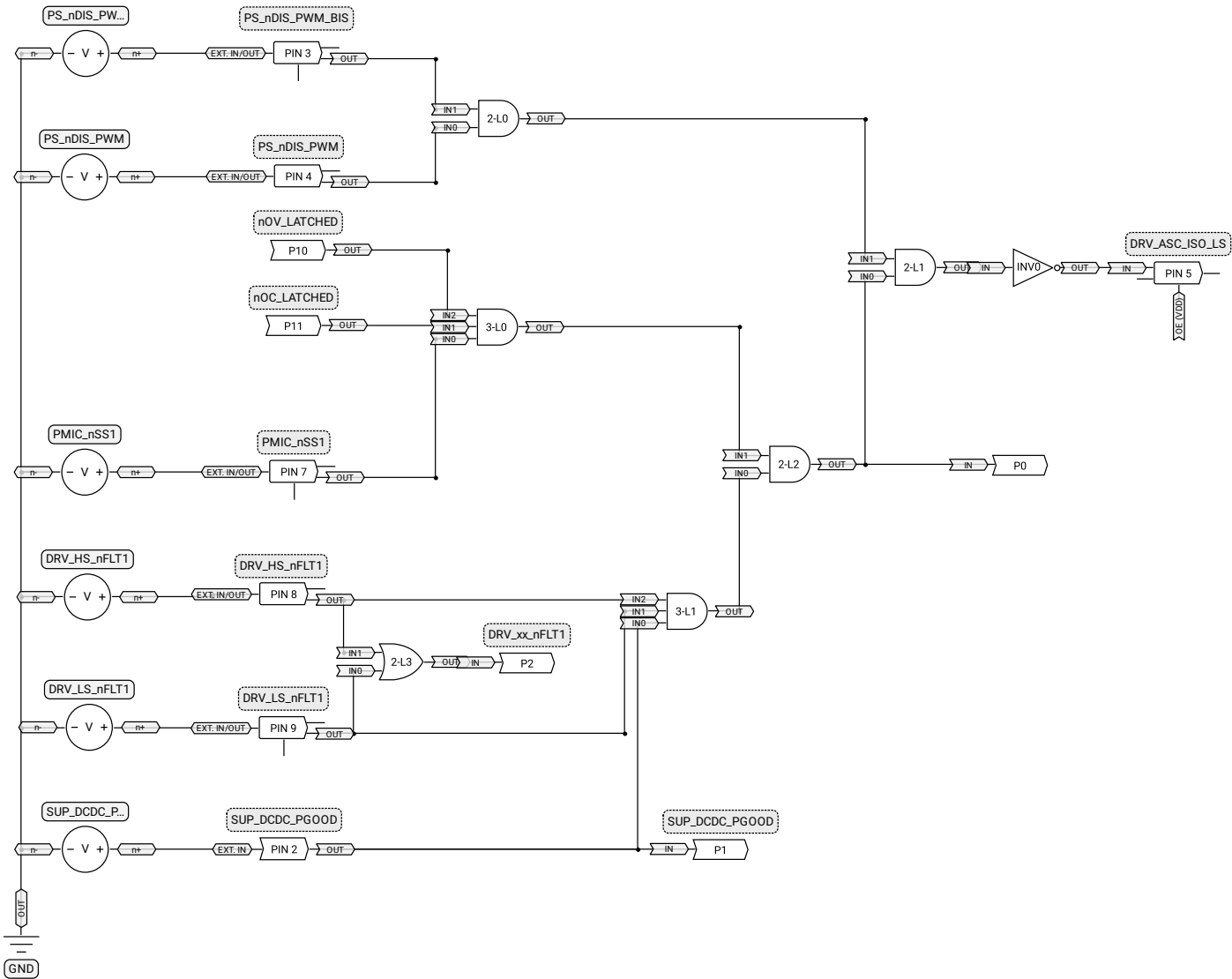
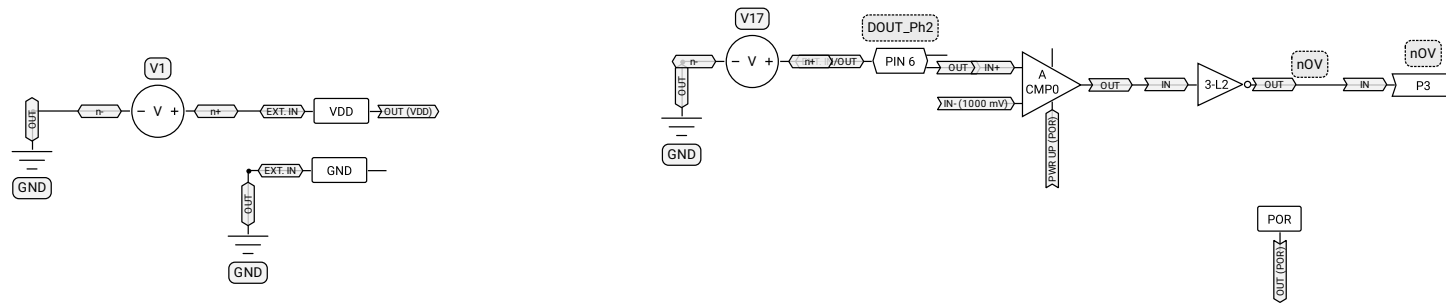
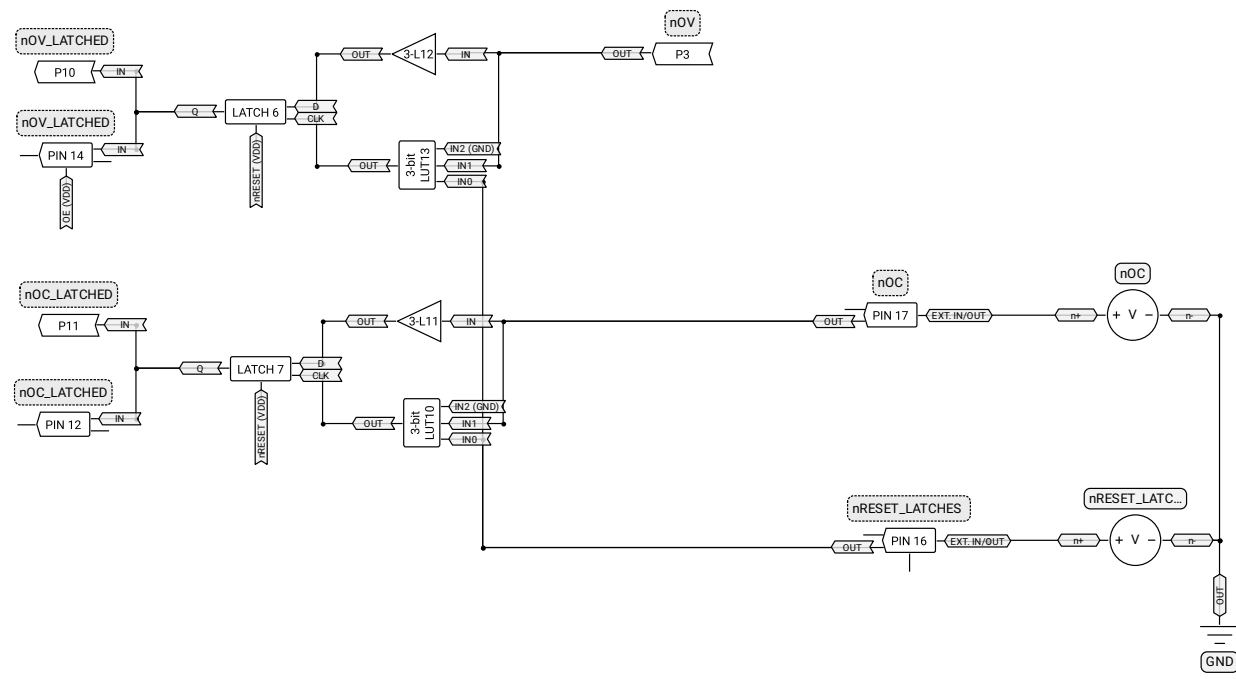
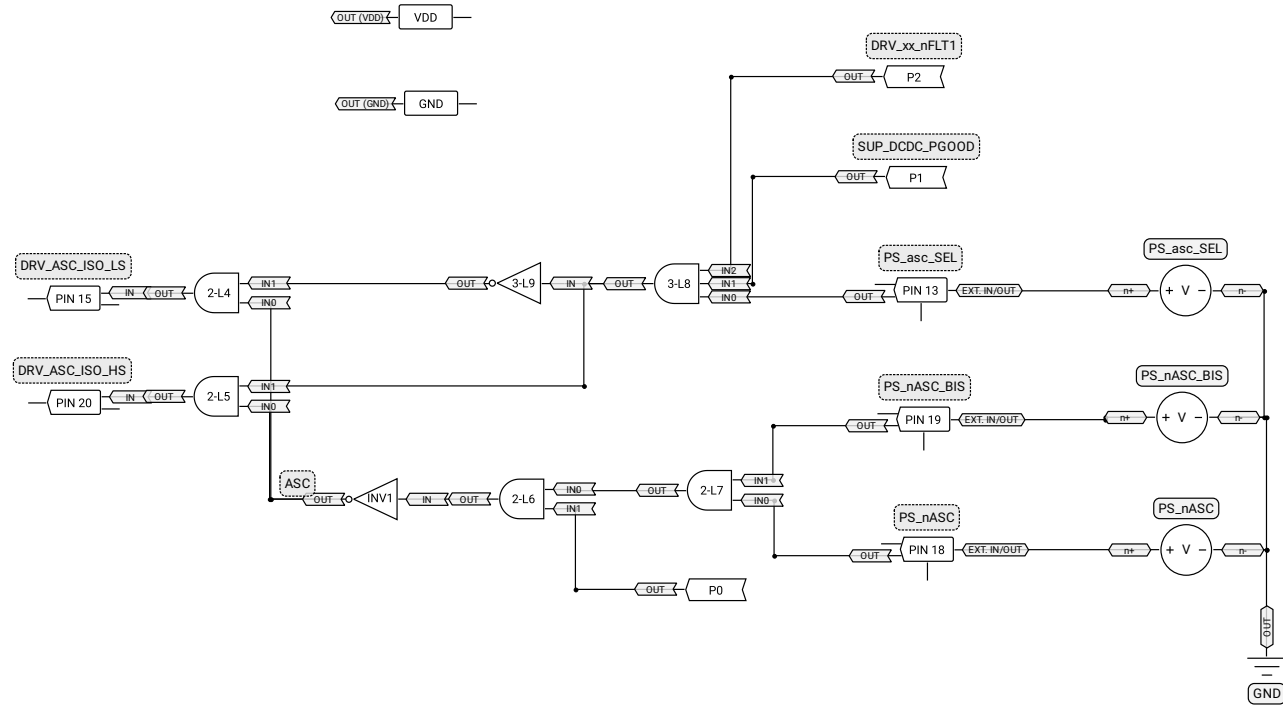


Matrix 0



Matrix 1



Matrix 0

VDD (PIN 1)

Property	Value
Min. value (V)	1.71
Typ. value (V)	3.30
Max. value (V)	5.00

PIN 2**Label: "SUP_DCDC_PGOOD"**

Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K
Reset mode	Disable

PIN 3**Label: "PS_nDIS_PWM_BIS"**

Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 4**Label: "PS_nDIS_PWM"**

Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 5**Label: "DRV_ASC_ISO_LS"**

Property	Value
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 6**Label: "DOUT_Ph2"**

Property	Value
I/O selection	Analog input/output
In mode	Analog input/output
Out mode	Analog input/output
Resistor	Floating

PIN 7**Label: "PMIC_nSS1"**

Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 8**Label: "DRV_HS_nFLT1"**

Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

PIN 9**Label: "DRV_LS_nFLT1"**

Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Up
Resistor value	10K

2-bit LUT0

IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Property	Value
Standard gates	AND

2-bit LUT1

IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Property	Value
Standard gates	AND

2-bit LUT2

IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Property	Value
Standard gates	AND

2-bit LUT3

<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0
0	1	1
1	0	1
1	1	1

*Property**Value*

Standard gates

OR

3-bit LUT0

<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

*Property**Value*

Standard gates

AND

3-bit LUT1

<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

*Property**Value*

Standard gates

AND

3-bit LUT2

<i>IN</i>	<i>OUT</i>
0	1
1	0

*Property**Value*

Standard gates

Inverter

A CMP0*Property**Value*

Hysteresis

Disable

Buffer bandwidth

1 kHz

Input current source

Disable

IN+ gain

Disable

IN+ source

PIN 6

IN- source

1000 mV

POR*Property**Value*

Chip power on delay

4 us

P1 (out)

Label: "SUP_DCDC_PGOOD"

P2 (out)

Label: "DRV_xx_nFLT1"

P3 (out)

Label: "nOV"

P10 (in)

Label: "nOV_LATCHED"

P11 (in)

Label: "nOC_LATCHED"

Matrix 1

VDD (PIN 1)	
Property	Value
Min. value (V)	1.71
Typ. value (V)	3.30
Max. value (V)	5.00

PIN 12 Label: "nOC_LATCHED"	
Property	Value
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 13 Label: "PS_asc_SEL"	
Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 14 Label: "nOV_LATCHED"	
Property	Value
I/O selection	Digital output
In mode	None
Out mode	1x push pull

PIN 15 Label: "DRV_ASC_ISO_LS"	
Property	Value
I/O selection	Digital output
In mode	None
Out mode	1x open drain PMOS
Resistor	Pull Down
Resistor value	10K

PIN 16 Label: "nRESET_LATCHES "	
Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 17 Label: "nOC"	
Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 18 Label: "PS_nASC"	
Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 19 Label: "PS_nASC_BIS"	
Property	Value
I/O selection	Digital input
In mode	Digital in without Schmitt trigger
Out mode	None
Resistor	Pull Down
Resistor value	1M

PIN 20 Label: "DRV_ASC_ISO_HS"	
Property	Value
I/O selection	Digital output
In mode	None
Out mode	1x open drain PMOS
Resistor	Pull Down
Resistor value	10K

2-bit LUT4		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1
Property		Value
Standard gates		AND

2-bit LUT5		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1
Property		Value
Standard gates		AND

2-bit LUT6		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1
Property		Value
Standard gates		AND

2-bit LUT7		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	0
1	1	1
Property		Value
Standard gates	AND	

3-bit LUT8			
<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1
<i>Property</i>		<i>Value</i>	
Standard gates		AND	

3-bit LUT9	
IN	OUT
0	1
1	0
Property	
Standard gates	Inverter

3-bit LUT10			
<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0
<i>Property</i>		<i>Value</i>	
Standard gates		Defined by user	

3-bit LUT11	
IN	OUT
0	0
1	1
Property	
Standard gates	Buffer

3-bit LUT12	
IN	OUT
0	0
1	1
Property	
Standard gates	Buffer

3-bit LUT13			
<i>IN2</i>	<i>IN1</i>	<i>IN0</i>	<i>OUT</i>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0
<i>Property</i>		<i>Value</i>	
Standard gates		Defined by user	

DFF/LATCH6	
Property	Value
Mode	LATCH
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

DFF/LATCH7	
Property	Value
Mode	LATCH
nSET/nRESET option	nRESET
Initial polarity	Low
Q output polarity	Non-inverted (Q)

P1 (in) Label: "SUP_DCDC_PGOOD"

P2 (in) Label: "DRV_xx_nFLT1"

P3 (in) Label: "nOV"

P10 (out)
Label: "nOV_LATCHED"

P11 (out)
Label: "nOC_LATCHED"

External Components

V1	
Property	Value
Element	Voltage Source
Internal capacitance	100nF
Internal resistance	100hm
Type	DC
DC Voltage	5V

PS_nDIS_PWM_BIS	
Property	Value
Element	Voltage Source
Type	DC
DC Voltage	3.3V

PS_nDIS_PWM	
Property	Value
Element	Voltage Source
Type	DC
DC Voltage	3.3V

PMIC_nSS1	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

PMIC_nSS1 Pattern Points	
Duration	Voltage
500µs	3.3V
500µs	3.3V
500µs	0V
500µs	0V
500µs	0V
500µs	3.3V
500µs	0V
500µs	0V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	3.3V
500µs	3.3V
500µs	3.3V
500µs	3.3V
500µs	3.3V
500µs	3.3V

DRV_HS_nFLT1	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

DRV_HS_nFLT1 Pattern Points	
Duration	Voltage
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	3.3V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	0V
500µs	3.3V
500µs	0V
500µs	3.3V

DRV_LS_nFLT1	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1µs
Fall time	1µs

PS_nASC_BIS	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Logic pattern
Mode	Normal
Umax	5V
Umin	0V

[illegible]

PS_nASC	
<i>Property</i>	<i>Value</i>
Element	Voltage Source

nOC	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1μs
Fall time	1μs

[illegible]

nRESET_LATCHES	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Internal capacitance	100nF
Internal resistance	100hm
Repeat state	Cyclic
Pre-start state	Low
Type	Logic pattern
Mode	Normal
Umax	3.3V
Umin	0V
Levels adjustment	Standard
Rise time	1μs
Fall time	1μs

V17	
Property	Value
Element	Voltage Source
Pre-start delay	0s
Repeat state	Cyclic
Pre-start state	Low
Type	Trapeze
Mode	Normal
Umin	0V
Umax	3.3V
T low	5ms
T rising	5ms
T high	5ms
T falling	5ms

Project Specs			
	Min.	Typ.	Max.
VDD	1.71	3.30	5.00
Temperature (°C):	-40.00	25.00	125.00

General Settings	
Power Supply Control mode	Regulator always ON and Charge Pump is automatically ON/OFF (use for dynamic 1.71V < VDD < 5.0V)
GPIO quick charge	Disable
Pattern ID	1
Lock status	Unlocked