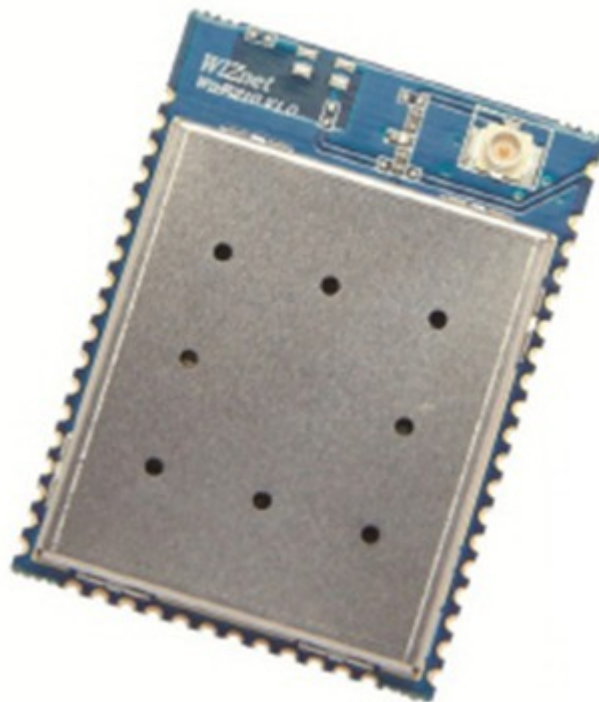


## WizFi210/220 Hardware design guide



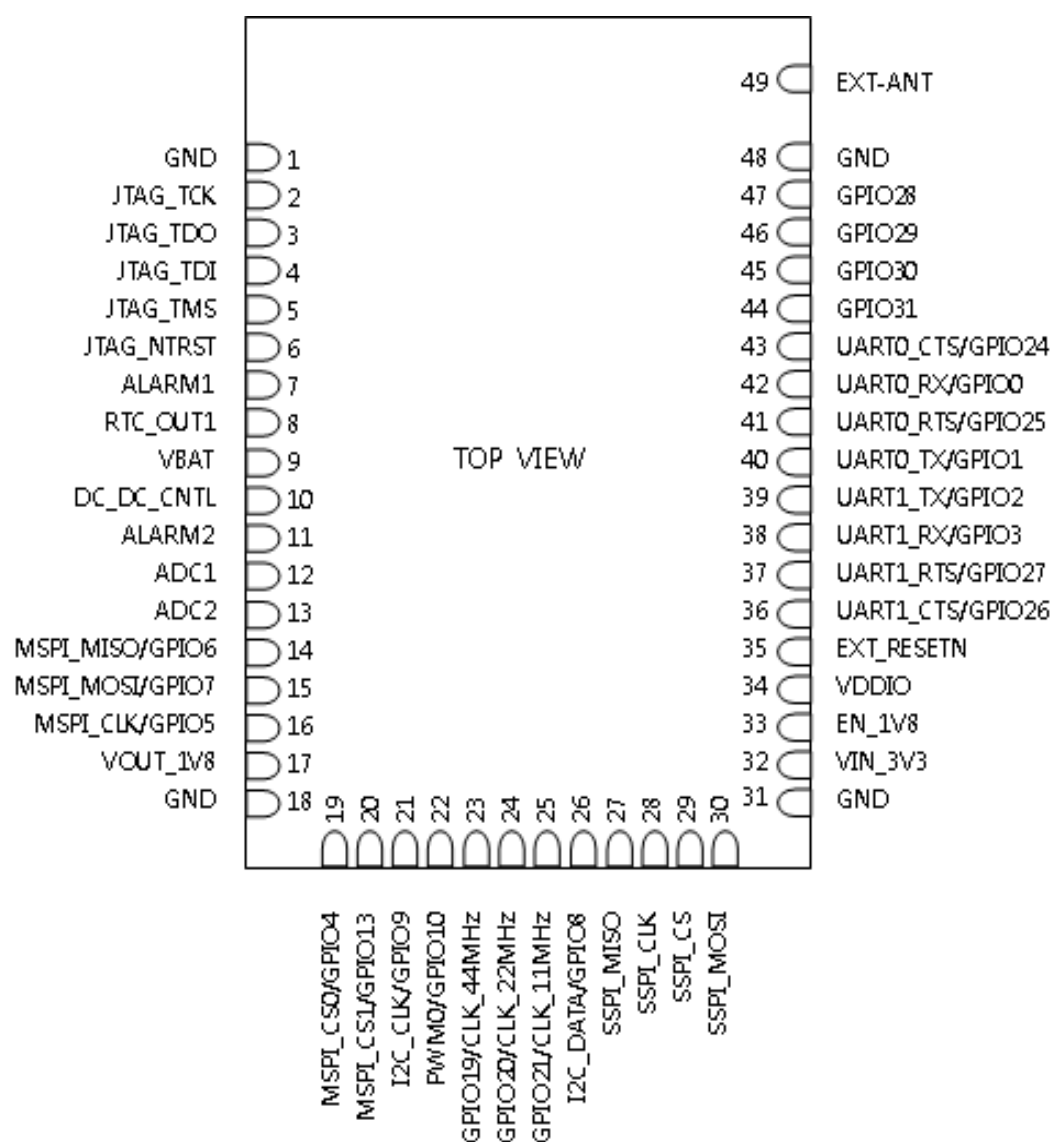
## 1. DEVICE NAME

WizFi210 / WizFi220

## 2. FUNCTION

Serial/SPI to WiFi Module

### 2.1 Pin assignment



( TOP VIEW )

## 2.2 Pin description

PIN	NAME	I/O	IN BIAS	DESCRIPTION
1	GND	P	NA	Ground
2	JTAG_TCK (*)	I	Pull-up	Joint Test Action Group Test Clock
3	JTAG_TDO (*)	O	NA	Joint Test Action Group Test Data Out
4	JTAG_TDI (*)	I	Pull-up	Joint Test Action Group Test Data In
5	JTAG_TMS (*)	I	Pull-up	Joint Test Action Group Test Mode Select
6	JTAG_NTRST (*)	I	Pull-up	Joint Test Action Group Test Mode Reset Active Low
7	ALARM1	I	Pull-down	Embedded Real Time Clock Wake Up Input 1
8	RTC_OUT1 (*)	O	NA	Embedded Real Time Clock Wake Up Output 1
9	VBAT	P	NA	Embedded Real Time Clock Power Supply
10	DC_DC_CNTL	O	NA	VIN_3V3 Regulator Control Output
11	ALARM2 (*)	I	Pull-down	Embedded Real Time Clock Wake Up Input 2
12	ADC1 (*)	I	NA	General Analog to Digital Converter 1
13	ADC2 (*)	I	NA	General Analog to Digital Converter 2
14	MSPI_MISO / GPIO6 (*)	I	Pull-down	Master Serial Peripheral Interface Bus Data Input / General Purpose Input Output
15	MSPI_MOSI / GPIO7 (*)	O	Pull-down	Master Serial Peripheral Interface Bus Data Output / General Purpose Input Output
16	MSPI_CLK / GPIO5 (*)	O	Pull-down	Master Serial Peripheral Interface Bus Clock / General Purpose Input Output
17	VOOUT_1V8 (*)	P	NA	Internal 1.8V Vout
18	GND	P	NA	Ground
19	MSPI_CS0 / GPIO4 (*)	O	Pull-down	Master Serial Peripheral Interface Bus Chip Select 0 / General Purpose Input Output
20	MSPI_CS1 / GPIO13 (*)	O	Pull-down	Master Serial Peripheral Interface Bus Chip Select 1 / General Purpose Input Output
21	I2C_CLK / GPIO9 (*)	IO	Pull-down	Inter-Integrated Circuit Clock / General Purpose Input Output

22	PWM0 / GPIO10	O	Pull-down	Pulse Width Modulator / General Purpose Input Out-put
23	GPIO19 / CLK_44MHz (*)	I	Pull-down	Internal Clock Circuitry Test Point / General Purpose Input Output
24	GPIO20 / CLK_22MHz (*)	I	Pull-down	Internal Clock Circuitry Test Point / General Purpose Input Output
25	GPIO21 / CLK_11MHz (*)	I	Pull-down	Internal Clock Circuitry Test Point / General Purpose Input Output
26	I2C_DATA / GPIO8 (*)	IO	Pull-down	Inter-Integrated Circuit Data / General Purpose Input Output
27	SSPI_MISO (*)	O	Pull-up	SPI Slave Transmit Data Output to the HOST
28	SSPI_CLK (*)	I	Pull-up	SPI Slave Clock Input from the HOST
29	SSPI_CS (*)	I	Pull-up	SPI Slave Chip Select Input from the HOST
30	SSPI_MOSI (*)	I	Pull-down	SPI Slave Receive Data Input from the HOST
31	GND	P	NA	Ground
32	VIN_3V3	P	NA	Single Supply Port
33	EN_1V8	I	NA	Internal 1.8V regulator enable port-Active High
34	VDDIO(**)	P	NA	All I/O voltage domain (can be tied to VIN_3V3 or tied to HOST I/O supply)
35	EXT_RESETN (*)	IO	Pull-up	Ext Reset Output and Module Reset Input for ARM Debugger. If you will use ARM Debugger, Connect EXT_RESETN(35) to JTAG_TRSTN(6) thru 0-ohm resistor.
36	UART1_CTS / GPIO26 (*)	I	Pull-down	Universal Asynchronous Receiver Transmitter 1 Clear to Send Input / General Purpose Input Output
37	UART1_RTS / GPIO27	O	Pull-down	Universal Asynchronous Receiver Transmitter 1 Request to Send Output / General Purpose Input Out-put / Firmware Program Mode
38	UART1_RX / GPIO3 (*)	I	Pull-down	Universal Asynchronous Receiver Transmitter 1 Receive Input / General Purpose Input Output

39	UART1_TX / GPIO2 (*)	O	Pull-down	Universal Asynchronous Receiver Transmitter 1 Transmitter Output / General Purpose Input Output
40	UART0_TX / GPIO1	O	Pull-down	Universal Asynchronous Receiver Transmitter 0 Transmitter Output / General Purpose Input Output
41	UART0_RTS / GPIO25	O	Pull-down	Universal Asynchronous Receiver Transmitter 0 Request to Send Output / General Purpose Input Out-put
42	UART0_RX / GPIO0	I	Pull-down	Universal Asynchronous Receiver Transmitter 0 Receive Input / General Purpose Input Output
43	UART0_CTS / GPIO24	I	Pull-down	Universal Asynchronous Receiver Transmitter 0 Clear to Send Input / General Purpose Input Output
44	GPIO31	IO	Pull-down	General Purpose Input Output
45	GPIO30	IO	Pull-down	General Purpose Input Output
46	GPIO29	IO	Pull-down	General Purpose Input Output
47	GPIO28	IO	Pull-down	General Purpose Input Output
48	GND	P	NA	Ground
49	EXT-ANT	IO	NA	External Antenna pad

(\*) is not available in this version.

(\*\*) To allow for design flexibility and support for multiple sensors with different voltages, the VDDIO banks are split, such that some of the VDDIO banks can be 1.8 V and some can be 3.3 V. If a VDDIO bank is connected to 1.8 V then the corresponding I/O signals for that bank should be driven at the same voltage.

VDDIO Bank 1 : GPIO28~29, JTAG,

VDDIO Bank 2 : SPI1(Master), Misc

VDDIO Bank 3 : GPIO18~23, PWM

VDDIO Bank 4 : I2C, SPI2(Slave), GPIO16~17

VDDIO Bank 5 : UART0~1

VDDIO Bank 6 : GPIO30~31

### 3. ELECTRICAL SPECIFICATION

#### 3.1 Absolute maximum ratings

Parameter	Min	Typ	Max	Unit
Storage temperature	-55		+125	°C
Supply Voltage (Vdd18)	-0.5		2.2	V
Supply Voltage (Vdd33)	-0.5		4.0	V

- Vdd18 refers to voltages supplied to pins identified as Vdd\_rf, Vdd\_adc, Vdd\_core.
- Vdd33 refers to voltages supplied to pins identified as Vdd\_sw, Vdd\_rtc, Vdd\_io

#### 3.2 Operating conditions

Parameter	Min	Typ	Max	Unit
Operating Ambient Range	-40		+85	°C
RTC Supply Voltage	1.2	3.3	3.6	V
CORE Supply Voltage	1.7	1.8	1.9	V
Single Supply Voltage	3.0	3.3	3.6	V

#### 3.3 Digital input specifications

Parameter	Min	Typ	Max	Unit
IO Supply Voltage	1.62 / 3	1.8 / 3.3	1.98 / 3.63	V
Input Low Voltage ( $V_{IL}$ )	-0.3		$0.25V_{DDIO}$	V
Input High Voltage ( $V_{IH}$ )	$0.8V_{DDIO}$		$V_{DDIO}$	V
Schmitt trig. Low to High threshold point ( $V_{T+}$ )	1.5			V
Schmitt trig. High to Low threshold point ( $V_{T-}$ )			1	V

#### 3.4 Digital output specifications

Parameter	Min	Typ	Max	Unit
IO Supply Voltage	1.62 / 3	1.8 / 3.3	1.98 / 3.63	V
Output Low Voltage ( $V_{OL}$ )	0		0.4	V
Output High Voltage ( $V_{OH}$ )	1.3		$V_{DDIO}$	V

Output rise time ( $t_{TLH}$ )			7	ns
Output fall time ( $t_{THL}$ )			7	ns

### 3.5 I/O digital specifications (Tri-state)

Parameter	Min	Typ	Max	Unit
IO Supply Voltage	1.62/3	1.8/3.3	1.98/3.63	
Input Low Voltage ( $V_{IL}$ )	-0.3		$0.25V_{DDIO}$	V
Input High Voltage ( $V_{IH}$ )	$0.8V_{DDIO}$		$V_{DDIO}$	V
Schmitt trig. Low to High threshold point ( $V_{T+}$ )	1.5			V
Schmitt trig. High to Low threshold point ( $V_{T-}$ )			1	V
Pull-Up Resistor ( $R_u$ )	0.05		1	M $\Omega$
Pull-Down Resistor ( $R_d$ )	0.05		1	V
Output Low Voltage ( $V_{OL}$ )	0		0.4	V
Output High Voltage ( $V_{OH}$ )	1.3		$V_{DDIO}$	ns
Output rise time @ 3.3V ( $t_{ToLH}$ )			7	ns
Output fall time @ 3.3V ( $t_{ToHL}$ )			7	ns
Input rise time ( $t_{TiLH}$ )			7	ns
Input fall time ( $t_{TiHL}$ )			7	ns

### 3.6 RTC input specifications

Parameter	Min	Typ	Max	Unit
RTC Supply Voltage ( $V_{DDRTC}$ )	1.2		3.6	V
Input Low Voltage ( $V_{IL}$ )	-0.3		$0.25V_{DDRTC}$	V
Input High Voltage ( $V_{IH}$ )	$0.8V_{DDRTC}$		$V_{DDRTC}$	V
Schmitt trig. Low to High threshold point ( $V_{T+}$ )	$0.57V_{DDRTC}$		$0.68V_{DDRTC}$	V
Schmitt trig. High to Low threshold point ( $V_{T-}$ )	$0.27V_{DDRTC}$		$0.35V_{DDRTC}$	V

### 3.7 RTC output specifications

Parameter	Min	Typ	Max	Unit
RTC Supply Voltage ( $V_{DDRTC}$ )	1.2		3.6	V
Output Low Voltage ( $V_{OL}$ )	0		0.4	V
Output High Voltage ( $V_{OH}$ )	$0.8V_{DDRTC}$		$V_{DDRTC}$	V
Output rise time ( $t_{TLH}$ )	19		142	ns
Output fall time ( $t_{THL}$ )	21		195	ns

### 3.8 Internal 1.8V regulator specifications

Parameter	Min	Typ	Max	Unit
Output Voltage ( $V_{OUT\_1V8}$ )		1.8		V
Maximum Output Current ( $I_{VOUT\_1V8}$ )		250	300	mA
1.8V Regulator Enable "H" Voltage ( $EN\_1V8$ )	1.0		$V_{IN\_3V3}$	V
1.8V Regulator Enable "L" Voltage ( $EN\_1V8$ )	0		0.25	V

### 3.9 Power consumption ( $V_{DD}=3.3V$ , $V_{DDIO}=1.8V$ , Temp= $25^{\circ}C$ )

WizFi210 / WizFi220	Min	Typ	Max	Unit
Standby mode (Only $V_{DDRTC}$ is active)		35	50	$\mu A$
Idle mode (CPU running, WLAN disconnected)			10 / 12	mA
Receive (-81dBm RX sens. @11Mbps)		125	130	mA
Transmit (+8dBm at antenna port @11Mbps)		135 / 250	140 / 260	mA

### 3.10 Power consumption ( $V_{DD}=3.3V$ , $V_{DDIO}=3.3V$ , Temp= $25^{\circ}C$ )

WizFi210 / WizFi220	Min	Typ	Max	Unit
Standby mode (Only $V_{DDRTC}$ is active)		35	50	$\mu A$
Idle mode (CPU running, WLAN disconnected)			11 / 13	mA



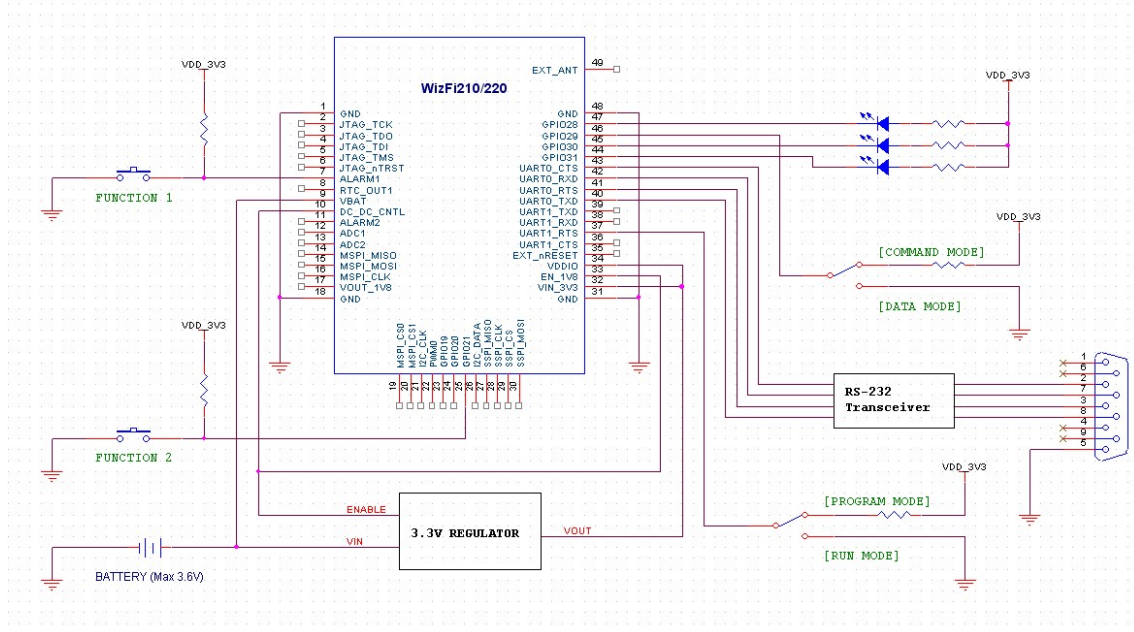
<b>Receive</b> (-81dBm RX sens. @11Mbps)		125	130	mA
<b>Transmit</b> (+8dBm at antenna port @11Mbps)		135 / 250	140 / 260	mA

### 3.11 RF specifications

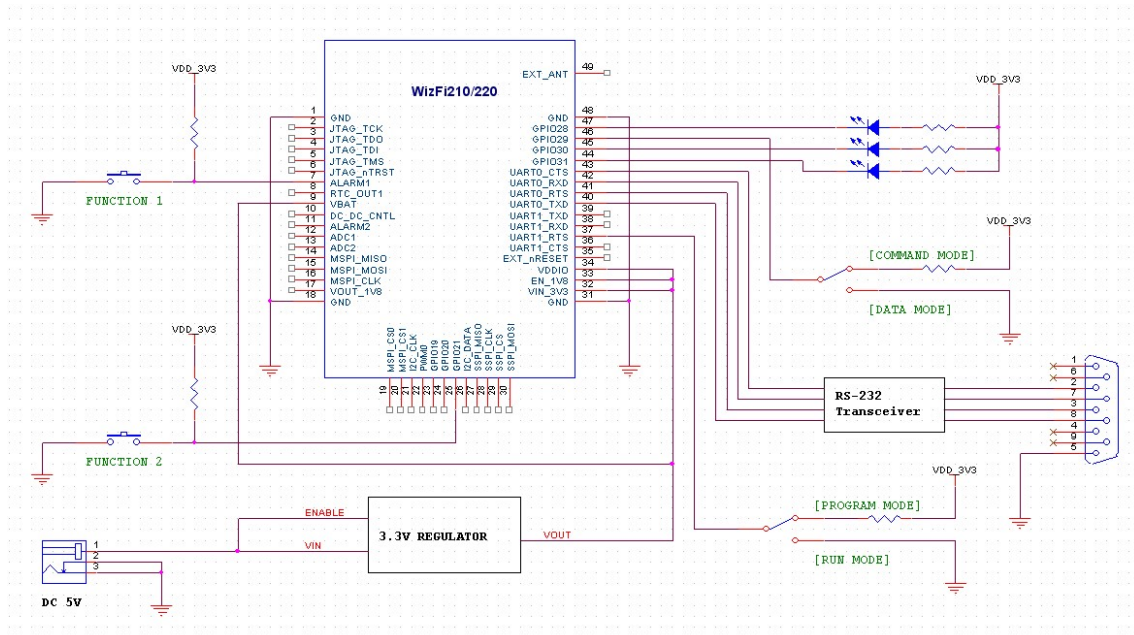
Specification	Description
<b>Modulation Technique</b>	DSSS for 1, 2Mbps CCK for 5.5, 11Mbps
<b>Data Rate</b>	IEEE 802.11b: 1, 2, 5.5 and 11Mbps
<b>Receive Sensitivity</b>	-84dBm $\pm$ 1dB @ 11Mbps -88dBm $\pm$ 1dB @ 5.5Mbps -90dBm $\pm$ 1dB @ 2Mbps -94dBm $\pm$ 1dB @ 1Mbps
<b>Transmit power (Average)</b>	WizFi210 : 8dBm $\pm$ 1dB @ 11Mbps WizFi220 : 17dBm $\pm$ 1.5dB @ 11Mbps
<b>Frequency Range</b>	USA: 2.400 ~ 2.483GHz Europe: 2.400 ~ 2.483GHz Japan: 2.400 ~ 2.497GHz China: 2.400 ~ 2.483GHz
<b>Operating Channels</b>	USA/Canada: 11 (1~11) Major Europe Countries: 13 (1~13) France: 4 (10~13) Japan: 14 for IEEE 802.11b (1~13 or 14th), 13 for IEEE 802.11g (1~13) Korea/China: 13 (1~13)
<b>Antenna</b>	U.FL External Antenna Support External Antenna Pad Support 1dBi Chip Antenna (Optional)

## 4. Basic reference schematics

### 4.1 $V_{IN}$ = Battery, Standby mode support



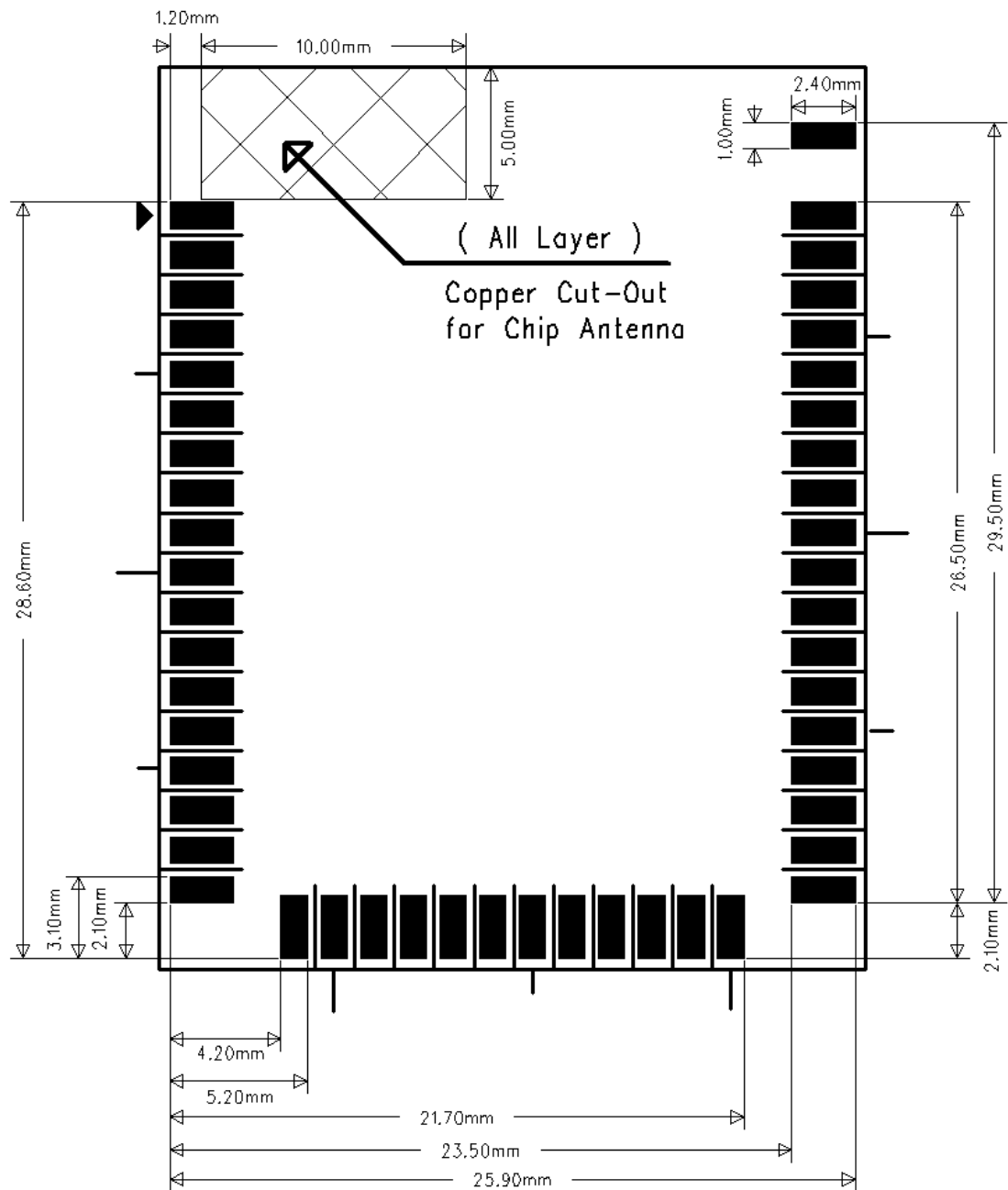
### 4.2 $V_{IN}$ = DC Adaptor, always active



- GPIO29 is used for mode transition between data and command mode.
- GPIO21 is used for factory reset and enable the limited AP mode. So, this should be considered, except in special cases
- In order to upgrade the firmware of the WIZFi210, the hardware design to transit between run mode and program mode is required as shown as above.

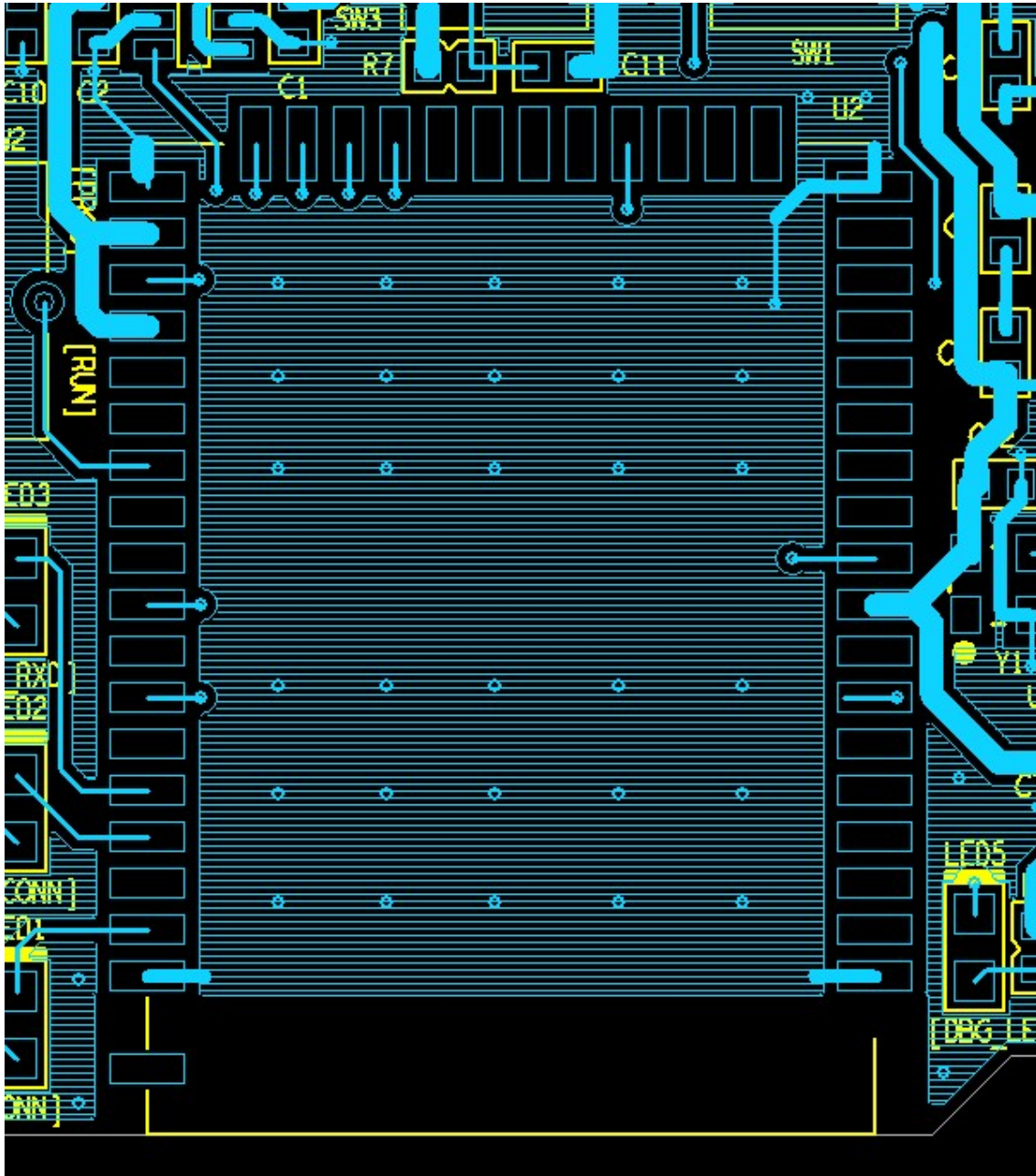


## 5.2 Recommended PCB Footprint

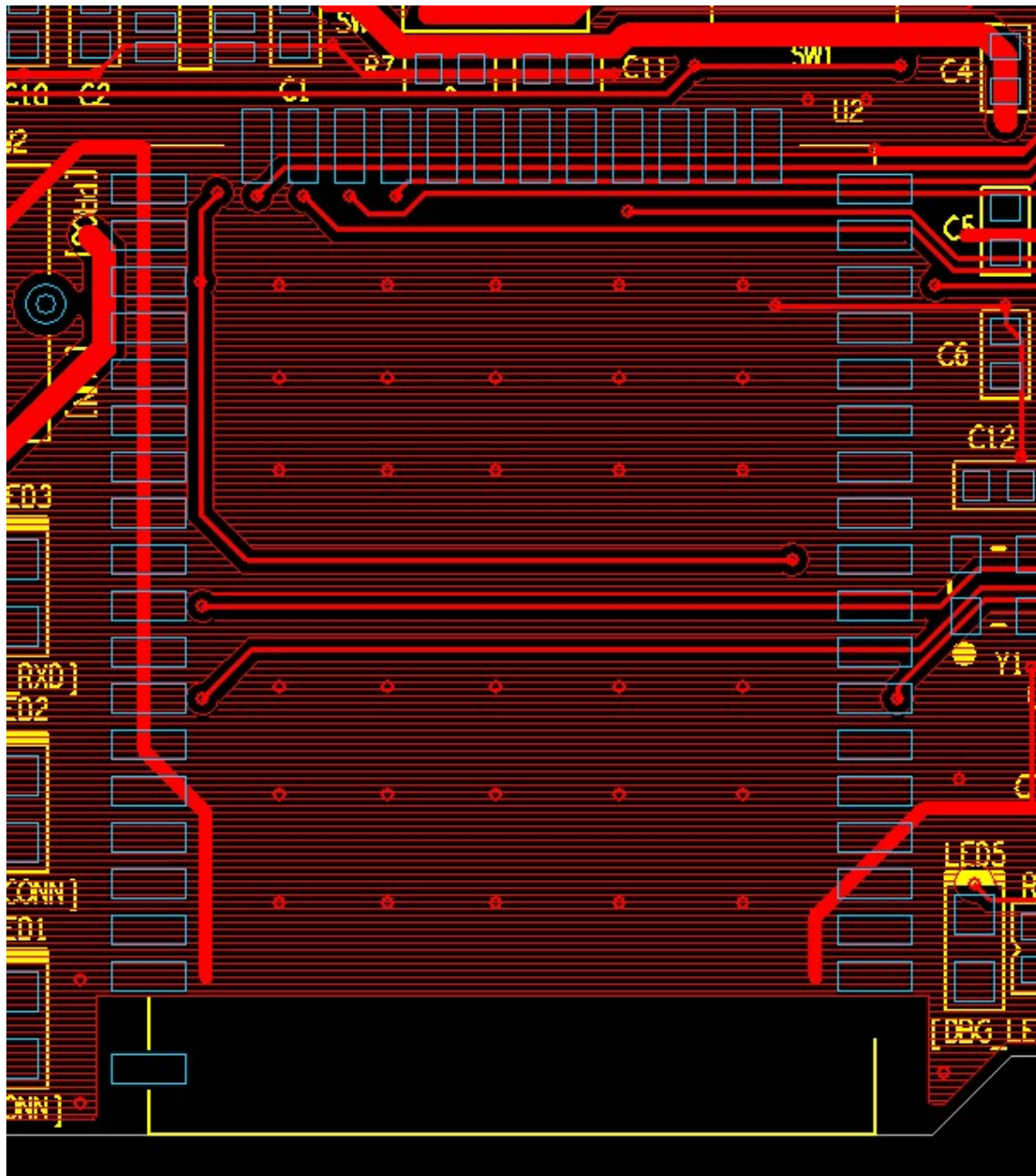


## 6. Reference layout design

### 6.1 Top layer design sample

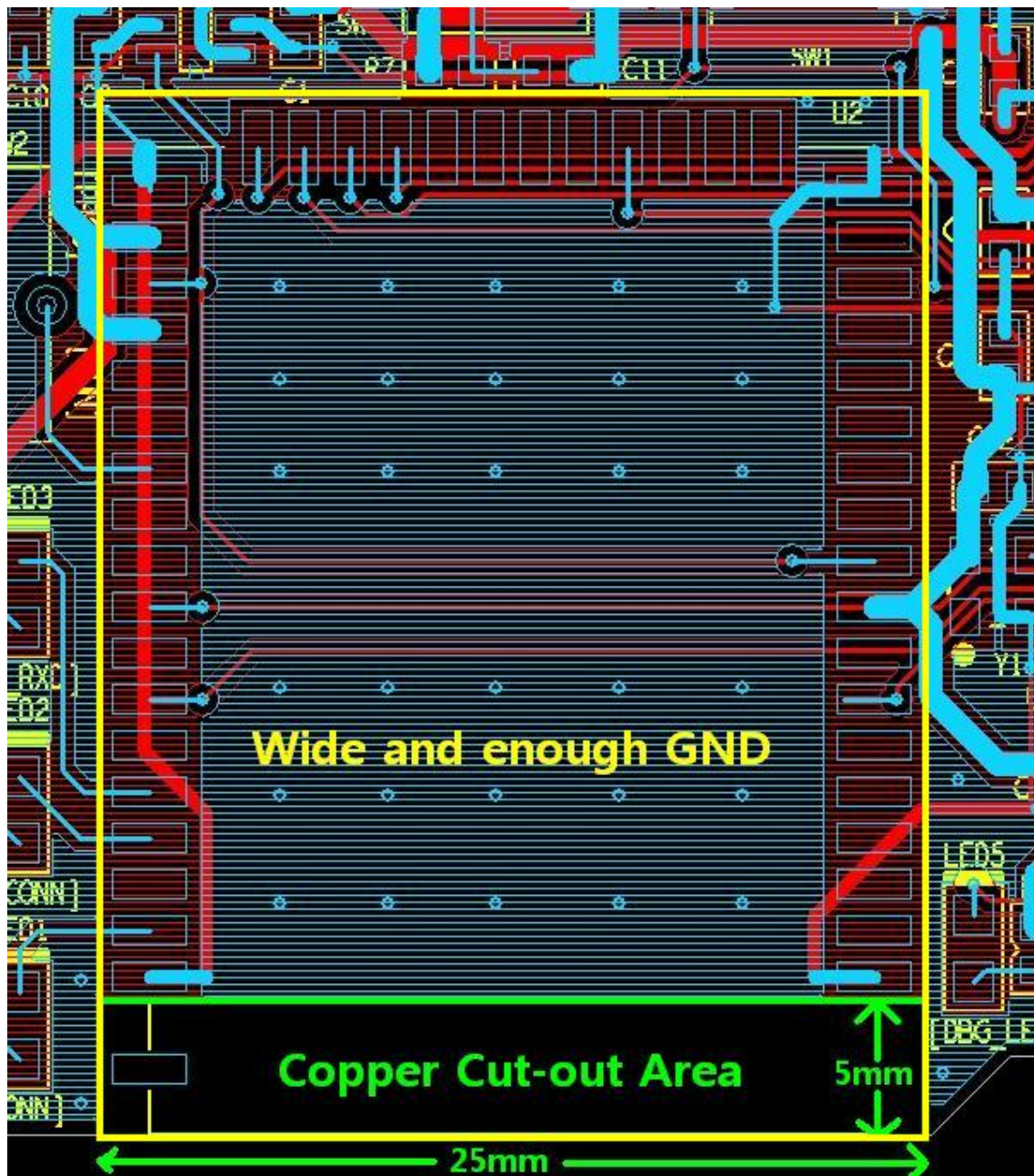


## 6.2 Bottom layer design sample





### 6.3 All layer design sample



## 7. IR REFLOW TEMPERATURE PROFILE

	Condition	Recommend	Range	Unit
Pre-Heat	Temperature Ramp up rate for (A)	3	2~4	°C/s
	Pre-heat time (B)	130	60~180	sec
	Pre-heat ending temperature (C)	200	150~200	°C
Heating	Peak Temperature range (D)	236	230~240	°C
	Melting time that is the time over 218°C (E)	45	30~50	sec

